CLAIMS

WE CLAIM:

1. A memory system having power backup comprising:

a backup supply line receiving a backup voltage when a line voltage is lost;

an electronically controlled switch;

volatile memory receiving voltage from the backup supply line controlled by the electronically controlled switch, the memory providing a low power operating mode controlled by volatile data held in the memory; and

a voltage supervisory circuit communicating with the backup supply line, the volatile memory, and the electronically controlled switch to operate the electronically controlled switch in response to a predetermined level in backup voltage below a normal backup voltage to disconnect the backup supply line from the volatile memory.

2. The memory system of claim 1 including further a backup voltage source connected to the backup supply line selected from the group consisting of a: battery, fuel cell, solar cell, generator, and capacitor.

3. The memory system of claim 1 further including a latching means connected between the voltage supervisory circuit and the electronically controlled switch whereby the electronically controlled switch is latched to disconnect the backup supply line from the volatile memory even after restoration of backup voltage to the normal backup voltage while the memory system is not receiving line voltage.

4. The memory system of claim 3 wherein the latch means is a logic gate having one input tracking the output of the controlled switch, that input remaining low while when the electronically controlled switch has disconnected the backup supply line from the volatile memory.

5. The memory system of claim 4 wherein the logic gate has a second input derived from the line power to cause the reconnection of the backup supply line to the volatile memory by the electronic switch when line power is present.

6. The memory system of claim 1 wherein the voltage supervisory circuit receives backup voltage from the backup supply line via the electronically controlled switch.

7. The memory system of claim 1 further including:

a microprocessor;

latching means connected between the voltage supervisory circuit and the microprocessor to provide a signal to the microprocessor indicating that the backup supply line has previously been disconnected from the volatile memory even after the backup supply line has been reconnected to the volatile memory while the memory system is not receiving line voltage;

whereby a control program executed on the microprocessor can determine after a power up the integrity of data in the volatile memory.

8. The memory system of claim 7 wherein the microprocessor executes the stored program to reset the latch after restoration of line power.

9. The memory system of claim 1 further including:

a microprocessor communicating with the volatile memory;

a low power warning circuit indicating a reduction of line power; and

wherein the microprocessor executes a control program to read a low power warning signal from the low power warning circuit and in response to that signal to write to the volatile memory the volatile data to put the volatile memory into the low power operating mode.

10. The memory system of claim 1 wherein the backup voltage is from a battery and further including a voltage conversion device connected between the battery and the volatile memory.

11. The memory system of claim 1 further wherein the volatile memory is dynamic random access memory.

12. A method of operating a memory system having a backup supply line providing backup voltage when a line voltage is lost, the memory system having an electronically controlled switch, a volatile memory receiving backup voltage from the backup supply line controlled by the electronically controlled switch, the volatile memory providing a low power operating mode controlled by volatile data held in the volatile memory; the method comprising the steps of:

(a) monitoring the voltage of the backup supply line; and

(b) in response to a predetermined level in backup voltage below a normal backup voltage, disconnecting the backup supply line from the volatile memory using the electronically controlled switch.

13. The method of claim 12 further including the step of connecting the backup supply line to a power source selected from the group consisting of a: battery, fuel cell, solar cell, generator, and capacitor.

14. The method of claim 12 including the step of latching a signal controlling the electronically controlled switch thereby disconnecting the backup supply line from the volatile memory even after restoration of backup voltage to the normal backup voltage.

15. The method of claim 12 including the step of unlatching the signal controlling the electronically controlled switch, thereby reconnecting the backup supply line to the volatile memory, after restoration of line voltage.

16. The method of claim 12 wherein the step of monitoring the voltage of the backup supply line is performed by a supervisory circuit receiving backup voltage from the backup supply line via the electronically controlled switch.

17. The method of claim 12 wherein the memory system further includes a microprocessor and including the step of latching a signal to the microprocessor indicating that the backup supply line has been disconnected from the volatile memory even after power from the backup supply line has been restored to the volatile memory while the memory system is not receiving line voltage.

18. The method of claim 17 including the step of unlatching the signal to the microprocessor the latch after restoration of line power.

19. The method of claim 12 including the steps of:

detecting a reduction of line power; and

in response to the reduction, writing to the volatile memory the volatile data to put the volatile memory into the low power operating mode.